ABSTRACT

The invention provides methods and logic for determining the source of a processor reset in a system having a processor and a plurality of processor reset sources. The plurality of processor reset sources couple to a corresponding plurality of RS latches. One of the RS latches sets in response to a processor reset generated by one of the processor resets. That one RS latch writes logic high to a dedicated register of a read register. After rebooting, the processor reads the read register to determine which register is logic high, corresponding to the source that generated the reset. The read register is reset by writing logic high into a write register, thereby resetting the set RS latch and clearing the logic high register of the read register. The processor writes logic low to all write register bits to clear enable the RS latches so that subsequent processor resets are identified.